ARM64 Conditional Selection Instructions

	condition **TRUE**	condition **FALSE**
CSEL Xd, Xa, Xb, condition	Xd = Xa	Xd = Xb
CSET Xd, condition	Xd = 1	Xd = 0
CSETM Xd, condition	Xd = 0x1111…	Xd = 0x0000…
CINC Xd, Xa, condition	Xd = Xa + 1	Xd = Xa
CINV Xd, Xa, condition	Xd = NOT(Xa)	Xd = Xa
CNEG Xd, Xa, condition	Xd = NOT(Xa)+1	Xd = Xa
CSINC Xd, Xa, Xb, condition	Xd = Xa	Xd = Xb + 1
CSINV Xd, Xa, Xb, condition	Xd = Xa	Xd = NOT(Xb)
CSNEG Xd, Xa, Xb, condition	Xd = Xa	Xd = NOT(Xb)+1

Each can use X or W registers, but not mixed in the same instruction.

conditions

	N	Z	C	V	
MI	1	–	–	–	negative
PL	0	–	–	–	positive/zero
EQ	–	1	–	–	equal
NE	–	0	–	–	not equal
VS	–	–	–	1	overflow
VC	–	–	–	0	no overflow
CS/HS	–	–	1	–	unsigned >=
CC/LO	–	–	0	–	unsigned <
HI	–	0	1	–	unsigned >
LS	–	1*	0*	–	unsigned <=
GE	=	–	–	=	signed >=
LT	≠	–	–	≠	signed <
GT	=	0	–	=	signed >
LE	≠*	1*	–	≠*	signed <=
AL	–	–	–	–	always

Flag states
1 flag set
0 flag clear
– ignored
= flags the same
≠ flags different
* either/both can be met

N = signed result is negative

Z = result is 0

C = add op ➜ overflow
sub op doesn't borrow
last bit shifted out when shifting

V = add/sub op ➜ signed overflow